A General Method to Model Full-Well Capacity for Anti-Blooming Pixels

Kaitlin M. Anagnost[1], Nathan Dougherty[2], Konstantin Loiko[1], Yvonne Lee[3], Michael Guidash[4], and Radu Ispasoiu[1]
[1]onsemi, 150 Rose Orchard Way, San Jose, CA 95134; [2]onsemi, 1401 N Kings Rd, Nampa, ID 83867; [3]onsemi, 4238 SW Research Way, Corvallis, OR 97333; [4]R M Guidash Consulting, 2185 Horizon Run, Lady Lake, FL 32162
Contact: Kaitlin.Anagnost@onsemi.com

Abstract

A general method for estimating the full-well capacity (FWC) of pixels with an anti-blooming (AB) path is proposed and explored to establish a FWC specification for automotive image sensors at different temperatures. While automotive image sensors must be operable at elevated temperatures, it is challenging to estimate the FWC before obtaining experimental data. The method presented here may provide an efficient means to determine/design FWC prior to running silicon. The FWC model is derived and analyzed, then the method used to obtain the key model parameters is presented. The method is applied to pixels with both different process conditions and layouts to demonstrate robustness.

Keywords—CMOS image sensor, automotive, anti-blooming, temperature, full-well, photodiode.

Introduction

There is a desire to establish a full-well capacity (FWC) specification for automotive image sensors at various temperatures due to the wide range of operating temperatures required. However, these pixels typically have anti-blooming (AB) structures to maximize dynamic range [1], complicating the modeling process. Several process and mask iterations are also usually required to optimize the pixel performance.

To address these challenges, a general method to predict the FWC of pixels with AB structures as a function of temperature and illumination is proposed. This model is applied to pixels with an AB path for which the cut-plane is illustrated in Fig. 1. As the photodiode fills up with charge, electrons can use the n-type AB path to overflow to the floating diffusion. This buried channel serves as a method to drain excess charge that would otherwise result in blooming, yielding a higher dynamic range in high-light scenarios.

The key terms impacting the FWC are the equilibrium full-well ($EFWC$), photocurrent (I_{ph}), transfer gate subthreshold current (I_{sub}) [2], and thermionic emission current of electrons over the AB barrier (I_{th})[3]. This model agrees with those discussed in [3]-[5], but in this work the model is applied to four pixels; three with different process conditions, and one with a different layout. Additionally, the effect of the thermionic emission current on the FWC across temperature is considered for the first time to the authors' knowledge.

The primary model parameters are determined via calculations and experimental measurements on similar pixels. The model is then verified via simulations and experiments using pixels with different process conditions and layouts to show versatility.

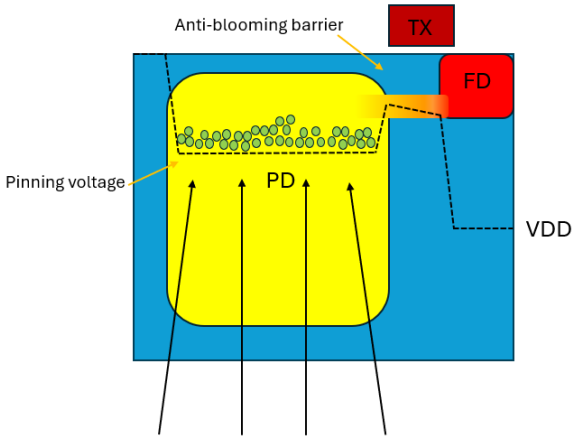

Figure 1. *Cartoon cut-plane of pixel with AB path showing the photodiode (PD), transfer gate (TX), and floating diffusion (FD).*

Model Derivation and Analysis

Qualitatively, FWC can be considered as the amount of charge in the pinned photodiode integrated from the pinning voltage (V_{pin}) to a minimum voltage (V_S) that keeps the charge trapped, as given by (1) in [4]:

$$FWC = \frac{1}{q}\int_{V_S}^{V_{pin}} C_{PPD}(V_{PPD})dV_{PPD} \qquad (1)$$

where C_{PPD} is the charge of the pinned photodiode, V_{PPD} is its potential, and q is the elementary charge. (1) may be rewritten as

$$FWC = \frac{1}{q}\int_{0}^{V_{pin}} C_{PPD}(V_{PPD})dV_{PPD} - \frac{1}{q}\int_{0}^{V_S} C_{PPD}(V_{PPD})dV_{PPD} \qquad (2)$$

The first term represents the full-well capacity at equilibrium, without the presence of light, or (4) in [4]:

$$EFWC(T) = \frac{1}{q}\int_{0}^{V_{pin}} C_{PPD}(V_{PPD})dV_{PPD}$$

$$= \frac{1}{q}\left(C_{PPD} \times V_{pin}(T)\right) \quad (3)$$

Simplifying the second term in (2),

$$\frac{1}{q}\int_0^{V_S} C_{PPD}(V_{PPD})dV_{PPD} = \frac{1}{q}V_S C_{PPD} \quad (4)$$

Plugging in (3) and (4) into (2) yields

$$FWC = EFWC - \frac{1}{q}V_S C_{PPD} \quad (5)$$

V_S must be greater than 0 V to prevent blooming [6].

To determine the FWC in the presence of illumination, first consider the equilibrium condition at full-well capacity:

$$I_{ph}(\Phi) = I_{sub}(T) + I_{th}(T) \quad (6)$$

Where I_{ph} is the photocurrent, I_{sub} is the transfer gate subthreshold current, and I_{th} is the thermionic emission current. The electron current into the photodiode, I_{ph} , balances the electron current out of the photodiode.

In pixels with AB structures, both the transfer gate subthreshold current I_{sub} and I_{th} may contribute to current out of the photodiode. (6) is similar to (6.29) in [7] but replaces the photodiode forward-bias leakage with I_{sub}. The forward bias injection of electrons from the photodiode to the substrate occurs only when I_{ph} is greater than the maximum I_{th} and I_{sub} which is a function of the physical dimensions of the transfer gate and the buried AB path, causing the photodiode potential to decrease further. This condition cannot be practically used in image capture. I_{sub} is an alternate path in cases where the transfer gate has a very low threshold voltage, and the gate is biased to provide dark current steering or an additional overflow path. However, I_{sub} may be excluded for pixels in which the transfer gate is sufficiently turned off during integration. I_{sub} may be estimated theoretically via (7.28) from [8]:

$$I_{sub}(T) = I_{dsat} \times \frac{W}{L} \times 10^{(V_{gs}-V_t)/S} \quad (7)$$

where I_{dsat} is the device's saturation current, $\frac{W}{L}$ is the transistor size, V_{gs} is the gate-source voltage when the transfer gate is in accumulation, V_t is the transfer gate threshold voltage, and S is the subthreshold slope.

I_{th} may be found using (109) from [9]:

$$I_{th}(T) = A^* T^2 e^{-q\varphi_b/kT} \quad (8)$$

where $A^* = \frac{4\pi q m^* k^2}{h^3}$; m^* is the effective mass and h is Planck's constant; and φ_b is the potential barrier height. $\varphi_b = V_S - V_{of}$, where V_S is the source voltage (minimum PD potential) and V_{of} is the overflow path potential [3].

Plugging (7) and (8) into (6),

$$I_{ph}(\Phi) = I_{dsat} \times \frac{W}{L} \times 10^{\frac{V_{gs}-V_t}{S}} + A^* T^2 e^{-q(V_S - V_{of})/kT} \quad (9)$$

V_S may now be found in (9) and plugged into (5) to find the FWC. The resulting equation was used to develop the method to estimate full-well capacity presented here.

Description of Method

The method used to obtain the model parameters in (9) and (5) is displayed in Fig. 2. First, the EFWC was found by measuring the pinning voltage across temperature and using TCAD to estimate C_{PPD}. Alternatively, V_{pin} may be estimated for pixels that have not yet been fabricated via TCAD or from equation (2) in [4]:

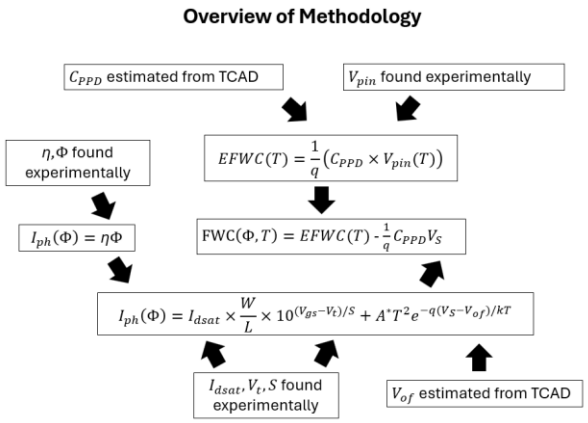

Figure 2*. Proposed model and methodology for estimating FWC vs. temperature and illumination.*

$$V_{pin}(T) \approx \frac{qN_{PPD}W_{PPD}^2}{2\epsilon_{Si}} - V_{bi}(T) \quad (10)$$

where N_{PPD} is the doping concentration of the buried channel, W_{PPD} is the buried channel depth, ϵ_{Si} is the Si permittivity, and $V_{bi}(T)$ is the built-in voltage of the upper junction [4].

I_{ph} is given in [4] as

$$I_{ph}(\Phi) = \eta\Phi \quad (11)$$

where η is the quantum efficiency and Φ is the incident photon flux [4]. η may be measured experimentally if silicon is available or estimated using a similar pixel's η. Φ is found from experimental conditions or optical simulations. The photocurrent may also be measured directly, as was done here, by sweeping the integration time and recording the responsivity if silicon is available.

I_{sub} and I_{th} were estimated theoretically using (7) and (8), respectively. I_{dsat}, V_t, and S were obtained via experimental measurements, while φ_b and V_{of} were estimated from TCAD.

These parameters can then be plugged into (9) and (5), respectively.

Model Comparison to TCAD

The FWC of a 3.0 µm automotive CIS pixel was simulated in TCAD under different temperatures and illuminations. The FWC was simulated by sweeping the integration time with fixed illumination level. The model and TCAD results are compared in Fig. 3 and show agreement in trend, but TCAD predicts larger FWCs at 80 C. Additionally, there was a slight mismatch in the input illumination photon flux values used in TCAD and the model, not shown. This misalignment is attributed to TCAD quantum efficiency calibration.

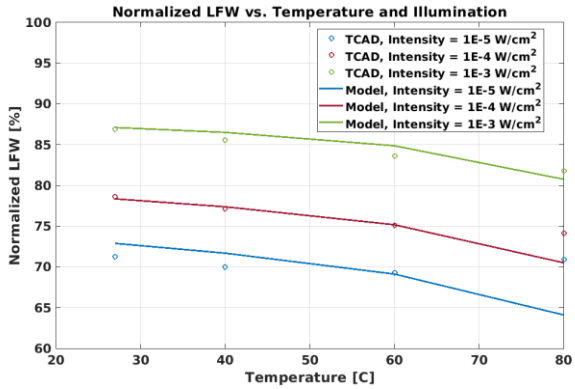

***Figure 3**. TCAD simulation and model results of FWC vs. temperature for three illumination levels.*

The FWC decreased with increasing temperature, as expected. This trend was caused by two factors competing against each other across temperature: The EFWC and $\frac{1}{q}V_S C_{PPD}$ term in (5). The EFWC grew due to V_{pin} increasing, in agreement with Fig. 4 of [4]. However, V_S increasing caused the second term to increase, outweighing the EFWC contribution and causing the FWC to decrease across temperature overall.

Model Comparison to Experimental Results

Since the model demonstrated proof-of-concept with TCAD simulations, experimental data for a similar 3.0 µm automotive CIS pixel were then obtained to compare against the model's predictions. The FWC of three wafers with the same pixel design but different implant conditions were measured experimentally under different temperatures and illuminations by sweeping the integration time with constant illumination level. The experimental results were then compared to the model's, as illustrated in Figures 4-6, and are in close agreement, except for minor discrepancies at 100 C. The FWC decreases with temperature in a similar fashion to the TCAD simulations in Fig. 3 but is much less dependent on illumination level. A smaller illumination range was used experimentally due to testing constraints, resulting in less variation in the measurements. The FWC decreased overall because the pixel's EFWC decreased with increasing temperature. The photodiode capacitance decreased at a faster rate than the pinning voltage increased with temperature, leading to a net decrease in EFWC.

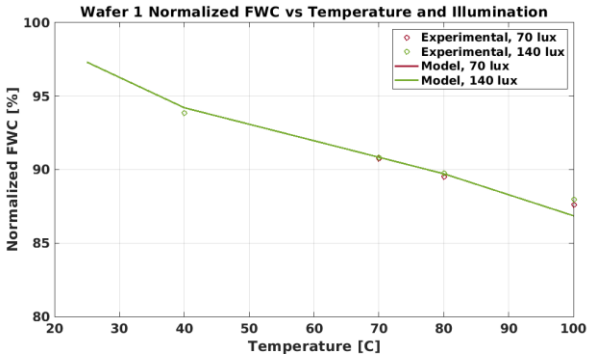

***Figure 4**. Experimental and model results of FWC vs. temperature for Wafer 1 for two illumination levels.*

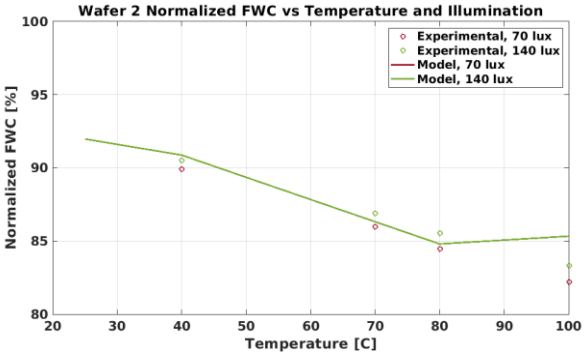

***Figure 5**. Experimental and model results of FWC vs. temperature for Wafer 2 for two illumination levels.*

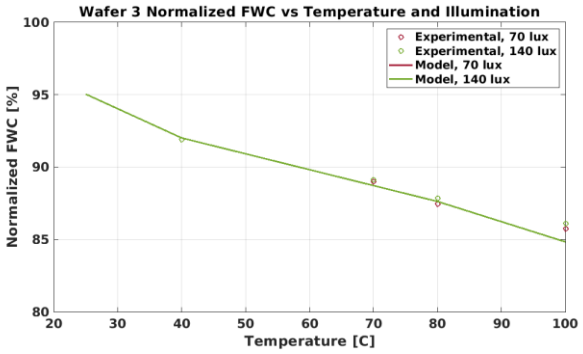

***Figure 6**. Experimental and model results of FWC vs. temperature for Wafer 3 for two illumination levels.*

The FWC of a 4.2 µm CIS pixel was also measured experimentally and compared to the model, as shown in Figure 7. The results are aligned despite this pixel

exhibiting significantly greater FWC drop across temperature than the three pixel variations measured previously. This match between the model and experimental results was achieved by considering the change in photodiode capacitance across temperature [9, 10]. This 4.2 μm pixel's EFWC decreases with increasing temperature more than those in Figs. 4-6 due to the photodiode depletion region width decreasing more across temperature.

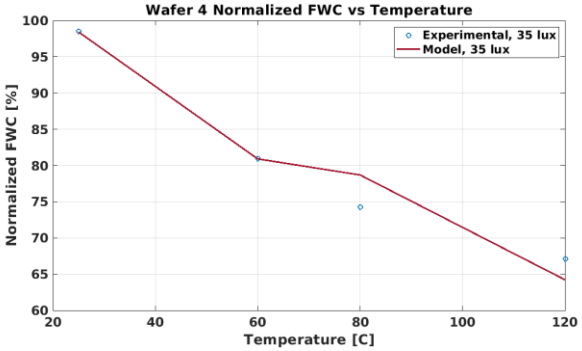

***Figure 7**. Experimental and model results of FWC vs. temperature for Wafer 4.*

Discussion

From these experiments, a method for better estimating the full-well capacity under various environmental conditions is obtained. The results indicate that this model is generally accurate for pixels with AB structures that exhibit both subtle and drastic FWC changes across temperature and illumination. This demonstrates that the model can be used across varied process conditions and layouts to provide an efficient means to determine/design FWC prior to running silicon. The primary drawback of the model and method is that a substantial amount of pixel characteristics like pinning voltage, photodiode capacitance, and thermionic emission current are required for the estimation. However, many of these parameters can be estimated beforehand using the equations shown here. Future work includes adding a model of the overflow collection FWC vs. illumination and temperature. More measurements using a wider range of illumination levels would also be of interest. If successful, a more accurate estimation for the charge-holding capacity of automotive CIS pixels will be gained.

Acknowledgments

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References

1. Takahashi, S., Huang, Y. M., Sze, J. J., Wu, T. T., Guo, F. S., Hsu, W. C., Tseng, T. H., Liao, K., Kuo, C. C., Chen, T. H., Chiang, W. C., Chuang, C. H., Chou, K. Y., Chung, C. H., Chouk, K. Y., Tseng, C. H., Wang, C. J., & Yaung, D. N. (2017). A 45 nm stacked CMOS image sensor process technology for submicron pixel. *Sensors (Switzerland)*, *17*(12). https://doi.org/10.3390/s17122816
2. Rabaey, J. M. (1995). *Digital Integrated Circuits: A Design Perspective*. Prentice Hall.
3. Miyauchi, K., Isozaki, T., Ikeno, R., & Nakamura, J. (2023). Analysis of Light Intensity and Charge Holding Time Dependence of Pinned Photodiode Full Well Capacity. *Sensors (Basel, Switzerland)*, *23*(21). https://doi.org/10.3390/s23218847
4. Pelamatti, A., Belloir, J. M., Messien, C., Goiffon, V., Estribeau, M., Magnan, P., Virmontois, C., Saint-Pé, O., & Paillet, P. (2015). Temperature Dependence and Dynamic Behavior of Full Well Capacity in Pinned Photodiode CMOS Image Sensors. *IEEE Transactions on Electron Devices*, *62*(4), 1200–1207. https://doi.org/10.1109/TED.2015.2400136
5. Pelamatti, A., Goiffon, V., Estribeau, M., Cervantes, P., & Magnan, P. (2013). Estimation and modeling of the full well capacity in pinned photodiode CMOS image sensors. *IEEE Electron Device Letters*, *34*(7), 900–902. https://doi.org/10.1109/LED.2013.2260523
6. Fossum, E. R., & Hondongwa, D. B. (2014). A review of the pinned photodiode for CCD and CMOS image sensors. *IEEE Journal of the Electron Devices Society*, *2*(3), 33–43. https://doi.org/10.1109/JEDS.2014.2306412
7. Pierret, R. F. (1996). *Semiconductor Device Fundamentals*. Addison-Wesley Publishing Company, Inc.
8. Hu, C. (2009). *Chapter 7: MOSFETs in ICs—Scaling, Leakage, and Other Topics* (pp. 259–289).
9. Sze, S. M., & Ng, K. K. (2007). Physics of Semiconductor Devices, 3rd Edition - Simon M. Sze, Kwok K. Ng. *Physics of Semiconductor Devices, 3rd Edition.; John Wiley & Sons, Inc.; NJ*.
10. Khan, U., & Sarkar, M. (2018). Dynamic Capacitance Model of a Pinned Photodiode in CMOS Image Sensors. *IEEE Transactions on Electron Devices*, *65*(7), 2892–2898. https://doi.org/10.1109/TED.2018.2831719